IPE JC87 MAY 2 0 2002 PATENT & TRADEMARK OFFICE

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IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF: :

MITSUHIRO YANO ET AL. : EXAMINER: CRANE, S.

SERIAL NO. 09/891,925

FILED: JUNE 27, 2001 : GROUP ART UNIT: 2811

RECEIVED MAY 21 2002 TECHNOLOGY CENTER 2800

FOR: SEMICONDUCTOR DEVICE AND: METHOD OF FABRICATING SAME

RESPONSE

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

In response to the Office Action of February 19, 2002, please amend the above-identified application as follows:

IN THE SPECIFICATION

Please replace the paragraph at column 1, lines 40-60, as follows:

Referring to FIG. 21, the semiconductor body 4 is initially formed, and the P^+ base layer 5, and P wells, P^+ layers serving as the guard rings 11 are formed in the surface of the N^- layer 3 of the semiconductor body 4. The gate insulating film 7 of silicon oxide is formed on the surface of the P^+ base layer 5, and a polysilicon film is formed on the surface of the gate insulating film 7. Then the N^+ emitter layer 6 and the channel stopper 15 are formed by diffusion, and the passivation films 12 and [17] 18 are formed. The gate interconnection line 9 and the emitter electrode 10 are formed as Al electrodes. Thereafter, the surface protective film 14 is formed to cover the IGBT surface except the emitter wire bonding region 13 and